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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.
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09/372,322 08/11/99 MIZUTANI

H NEM-01601

026339 MM91/0404
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EXAMINER

2817
ART UNIT PAPER NUMBER

2817
DATE MAILED:

04/04/01

Please find below and/or attached an Office communication concerning this application or proceeding.

Commissioner of Patents and Trad marks

Office Action Summary	Application No.	Applicant(s)
	09/372,322	MIZUTANI, HIROSHI
	Examiner Stephen E. Jones	Art Unit 2817

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136 (a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1) Responsive to communication(s) filed on 19 March 2001.
 2a) This action is FINAL. 2b) This action is non-final.
 3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4) Claim(s) 1-19 is/are pending in the application.
 4a) Of the above claim(s) 11-19 is/are withdrawn from consideration.
 5) Claim(s) _____ is/are allowed.
 6) Claim(s) 1-10 is/are rejected.
 7) Claim(s) _____ is/are objected to.
 8) Claims 1-11 are subject to restriction and/or election requirement.

Application Papers

9) The specification is objected to by the Examiner.
 10) The drawing(s) filed on 11 August 1999 is/are objected to by the Examiner.
 11) The proposed drawing correction filed on _____ is: a) approved b) disapproved.
 12) The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. § 119

13) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
 a) All b) Some * c) None of:
 1. Certified copies of the priority documents have been received.
 2. Certified copies of the priority documents have been received in Application No. _____.
 3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
 * See the attached detailed Office action for a list of the certified copies not received.
 14) Acknowledgement is made of a claim for domestic priority under 35 U.S.C. § 119(e).

Attachment(s)

15) Notice of References Cited (PTO-892) 18) Interview Summary (PTO-413) Paper No(s). _____.
 16) Notice of Draftsperson's Patent Drawing Review (PTO-948) 19) Notice of Informal Patent Application (PTO-152)
 17) Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____. 20) Other: _____

DETAILED ACTION

Election/Restrictions

1. Newly submitted claims 11-19 directed to an invention that is independent or distinct from the invention originally claimed for the following reasons:

Claims 11-19 are drawn to a semiconductor switch having specific layer materials classified in Class 257, which is independent or distinct from original Claims 1-9 which are drawn to a switch formed of co-planar transmission lines on a substrate classified in Class 333.

Since applicant has received an action on the merits for the originally presented invention, this invention has been constructively elected by original presentation for prosecution on the merits. Accordingly, claims 11-19 are withdrawn from consideration as being directed to a non-elected invention. See 37 CFR 1.142(b) and MPEP § 821.03.

Drawings

2. The drawings are objected to under 37 CFR 1.83(a) because they fail to show the "resistor" connected to the "third electrode", as recited in Claim 10 and as described in the specification. Any structural detail that is essential for a proper understanding of the disclosed invention should be shown in the drawing. MPEP § 608.02(d). Correction is required.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

4. Claims 1-9 are rejected under 35 U.S.C. 103(a) as being unpatentable over Fleming et al. of record in view of Streetman, ***Solid State Electronic Devices***.

Fleming et al. discloses coplanar transmission lines on a semiconductor substrate forming a switch including a center signal conductor electrode between two parallel electrodes which are grounded. The Fleming device is rendered off when the central conductor is zero-biased (see Fleming page 253-5, paragraph under Fig. 2) and is rendered on when the central conductor is supplied with a voltage. This design of a semiconductor device is considered in the art to be acting in the enhancement mode. Note that it is inherent that the center signal electrode includes terminals on its ends for signal input/output (see Fleming discussion, 1st paragraph under Experimental Results).

However, Fleming et al. does not disclose: the first electrode being a drain electrode of a transistor, the second electrode being a source electrode of said transistor, and the third electrode is a gate electrode of said transistor (Claims 2 and 6) (see Streetman Fig. 8-5, page 295); or that the switch is rendered on when the center conductor is supplied with ground and is rendered off when the center conductor is supplied with a non-zero voltage (Claims 1 and 5); or the first electrode being a first cathode electrode of a diode, the second electrode being a second cathode electrode of

said diode, and the third electrode is a anode electrode of said diode (Claims 3 and 7); or the first electrode being a first anode electrode of a diode, the second electrode being a second anode electrode of said diode, and the third electrode is a cathode electrode of said diode (Claims 4 and 8); or that the electrodes are formed on a substrate including an AlGaAs layer and an InGaAs layer (Claim 9).

Streetman, *Solid State Electronic Devices*, pages 300-301, 320-321, teaches the well-known equivalent depletion and enhancement mode semiconductors. The Streetman reference discloses that a depletion mode switch typically requires a negative gate voltage to turn the device off.

Regarding Claims 1 and 5, it would have been considered obvious to one of ordinary skill in the art to have modified the Fleming et al. device to function as a depletion mode semiconductor switch (such as taught by Streetman) instead of as a enhancement mode semiconductor device, because it would have been an art-recognized equivalent switching semiconductor device.

It would have been considered obvious to one of ordinary skill in the art to have used the coplanar transmission lines as taught by Fleming et al. to realize a variety of electronic devices: for example, to have the first electrode being a drain electrode of a transistor, the second electrode being a source electrode of said transistor, and the third electrode is a gate electrode of said transistor (Claims 2 and 6); or the first electrode being a first cathode electrode of a diode, the second electrode being a second cathode electrode of said diode, and the third electrode is a anode electrode of said diode (Claims 3 and 7); or the first electrode being a first anode electrode of a diode, the

second electrode being a second anode electrode of said diode, and the third electrode is a cathode electrode of said diode (Claims 4 and 8), because the diodes and transistors as mentioned are well-known in the art, and it would have been an art-recognized use for coplanar transmission lines.

Also, it would have been an obvious design choice to one of ordinary skill in the art to have formed the coplanar transmission lines as taught by Fleming et al. on a well-known semiconductor substrate such as one including an AlGaAs layer and an InGaAs layer (Claim 9) which would have been art-recognized equivalents to the disclosed GaAs substrate (i.e. heterojunctions are art-recognized equivalent to Schottky junction devices, see Streetman page 190).

5. Claim 10 is rejected under 35 U.S.C. 103(a) as being unpatentable over the previous rejection as applied to claims 1-9 above, and further in view of the admitted prior art Fig. 10.

The combination of Fleming et al. and Streetman as described in the previous rejection discloses coplanar transmission lines which function as a semiconductor device.

However, the combination of Fleming and Streetman does not disclose that the third electrode has a resistor connected to its first end for supplying the ground potential or non-zero potential (Claim 10).

The admitted prior art Fig. 13 discloses a well-known resistor for limiting current from a bias source.

One of ordinary skill in the art would have found it obvious to include a resistor connected to the end of the third electrode of the device taught by the combination of Fleming et al. and Streetman, because it is well-known to add a resistor to limit current from the bias source.

Response to Arguments

6. Applicant's arguments filed 3/19/01 have been fully considered but they are not persuasive.

Applicant argues that the Fleming device functions in an opposite manner from the present invention.

Also, applicant argues that the Fleming reference requires two power sources and that the present Claims 1 and 5 are in need of only one power source. This argument is not commensurate with what is claimed. Also, note that the Fleming reference discloses that the device can operate at zero-bias (see paragraph under Fig. 2).

With respect to the arguments concerning the Fleming et al. reference and what is well-known, these arguments are addressed in the rejections above and the Streetman reference is supplied as evidence to establish what is well-known.

Additionally with respect to the arguments concerning transistors and diodes, it should be recognized that the Fleming device may be considered a type of transistor (see Fig. 2 of Fleming in comparison with Streetman Fig. 8-5). The features of a transistor also inherently include features of a diode (i.e. Schottky barrier, see paragraph 2 of Fleming).

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Conclusion

7. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Stephen E. Jones whose telephone number is 703-305-0390. The examiner can normally be reached on Monday through Friday from 8 AM to 4 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Bob Pascal can be reached on 703-308-4909. The fax phone numbers for the organization where this application or proceeding is assigned are 703-305-0142 for regular communications and 703-305-0142 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.

sej
April 2, 2001



Justin P. Bettendorf
Primary Examiner
Art Unit 2817